AMENDMENTS TO THE CLAIMS

1. (original) A pixel circuit, comprising:

a first photodiode region having a first light sensitivity , said photodiode region being coupled to a first floating diffusion region through a transfer transistor;

a readout circuit, said readout circuit being coupled to the first floating diffusion region;

a second photodiode region having a second light sensitivity, said photodiode region being coupled to the first floating diffusion region through a connecting transistor; and

a capacitive element, said capacitive element being coupled to the second photodiode region, and further coupled to the readout circuit.

2. (currently amended) The pixel circuit of claim 1, wherein the readout circuit comprises a reset transistor, said reset transistor being ~~controllable to reset~~ configured for resetting the first floating diffusion region.

3. (original) The pixel circuit of claim 2, wherein the readout circuitry further comprises a source-follower transistor, said source-follower transistor having a source terminal coupled to said capacitive element, a gate terminal coupled to the drain terminal of the reset transistor, and a drain terminal coupled to a source terminal of a select transistor, said select transistor having a gate terminal coupled to a select line, and a drain terminal coupled to an output bus line.

4. (original) The pixel circuit of claim 1, wherein the capacitive element is a poly-insulator-poly type capacitor.

5. (original) The pixel circuit of claim 4, wherein the capacitance of said capacitor is in the range of 5 $fF/\mu m^2$ to 10 $fF/\mu m^2$.

6. (original) The pixel circuit of claim 1, wherein the first sensitivity is higher than the second sensitivity.

7. (original) The pixel circuit of claim 1, wherein the capacitance of the first floating diffusion region is less than the capacitance of the capacitive element.

8. (original) The pixel circuit of claim 1, wherein the first and second photodiode regions comprise pinned photodiodes.

9. (original) The pixel circuit according to claim 8, wherein a pinned potential is less than 1 volt.

10. (original) The pixel circuit of claim 1, wherein the first and second photodiode regions comprise buried photodiodes.

11. (original) The pixel circuit of claim 1, further comprising:

a third photodiode region having the first light sensitivity, said third photodiode region being coupled to a second floating diffusion region through a second transfer transistor, said second floating diffusion region being coupled to the first floating diffusion region;

a fourth photodiode region having the second light sensitivity, said fourth photodiode region being coupled to the second floating diffusion region through a second connecting transistor; and

a second capacitive element, said second capacitive element being coupled to the second low-sensitivity photodiode region, and further coupled to the readout circuit..

12. (original) A method of operating a pixel during a frame period, comprising:

resetting and sampling a floating diffusion region to obtain a first signal;

transferring charge from a first photodiode region having a first light sensitivity to the floating diffusion region, said charge being subsequently read out and sampled to obtain a second signal;

resetting the floating diffusion region;

transferring charge from a second photodiode region having a second light sensitivity to the floating diffusion region;

reading out and sampling the transferred charge to obtain a third signal;

resetting the floating diffusion region while charge is being transferred from the second photodiode region; and

reading out and sampling a remaining voltage to obtain a fourth signal prior to the end of the frame period.

13. (original) The method of claim 12, further comprising the step of subtracting the first signal from the second signal to obtain a first photodiode signal.

14. (original) The method of claim 13, wherein the first photodiode signal is a high sensitivity photodiode signal.

15. (original) The method of claim 12, further comprising the step of subtracting the third signal from the fourth signal to obtain a second photodiode signal.

16. (original) The method of claim 15, wherein the second photodiode signal is a low sensitivity photodiode signal.

17. (original) The method of claim 12, further comprising the step of resetting the first photodiode region and the floating diffusion region after the remaining voltage is read out, and before the end of the frame period.

18. (original) The method of claim 17, further comprising the step of resetting the second photodiode region and the floating diffusion region after the first photodiode region and the floating diffusion region are reset, and prior to the end of the frame period.

19. (original) A pixel circuit, comprising:

a first photodiode region having a first sensitivity characteristic, said first photodiode region being coupled to a floating diffusion node through a transfer transistor;

a second photodiode region having a second sensitivity characteristic, said second photodiode region being coupled to the floating diffusion node through a connecting transistor;

a reset transistor connected to and for resetting the floating diffusion region;

a readout circuit connected to and for reading out the voltage on the floating diffusion region; and

a capacitive element, said capacitive element being coupled to the second photodiode region, and further coupled to a voltage line.

20. (original) The pixel circuit of claim 19, wherein the capacitive element is a poly-insulator-poly type capacitor.

21. (original) The pixel circuit of claim 20, wherein the capacitance of said capacitor is in the range of 5 $fF/\mu m^2$ to 10 $fF/\mu m^2$.

22. (original) The pixel circuit of claim 19, wherein the first sensitivity characteristic is higher than the second sensitivity characteristic.

23. (original) The pixel circuit of claim 19 wherein the readout circuit comprises a source-follower transistor coupled to a select transistor, said source-follower transistor being further coupled to the reset transistor and to the voltage line, and said select transistor being further coupled to a select line and an output bus line.

24. (original) The pixel circuit of claim 19, wherein the pixel circuit further comprises:

a third photodiode region having said first sensitivity characteristic, said third photodiode region being coupled to a second floating diffusion node through a second transfer transistor, said second floating diffusion node being coupled to the floating diffusion node;

a fourth photodiode region having said second sensitivity characteristic, said low sensitivity photodiode region being coupled to the second floating diffusion node through a second connecting transistor; and

a second capacitor, said second capacitor coupled to the fourth photodiode region, and further coupled to the readout circuit.

25. (original) The pixel circuit of claim 24, wherein the first sensitivity characteristic is greater than the second sensitivity characteristic.

26. (original) A method of operating a pixel during a frame period, comprising the steps of:

resetting and sampling a floating diffusion region to obtain a first signal;

saturating a plurality of high-sensitivity photodiode regions to allow accumulated charge to flow to a plurality of low-sensitivity photodiode regions through said floating diffusion region;

reading out and sampling the charge on the plurality of low-sensitivity photodiode regions through the floating diffusion region to obtain a second signal;

resetting and sampling the floating diffusion region to obtain a third signal; and

reading out and sampling the charge on the plurality of high-sensitivity photodiode region through the floating diffusion region to obtain a fourth signal.

27. (original) The method of claim 26, further comprising the step of subtracting the first signal from the second signal to obtain a low-sensitivity photodiode signal.

28. (original) The method of claim 27, further comprising the step of subtracting the third signal from the fourth signal to obtain a high-sensitivity photodiode signal.

29. (original) The method of claim 26, further comprising the step of resetting the plurality of high-sensitivity photodiode region and the floating diffusion region after the remaining voltage is read out, and before the end of the frame period.

30. (original) The method of claim 29, further comprising the step of resetting the plurality of low-sensitivity photodiode region and the floating diffusion region are again reset after the plurality of high-sensitivity photodiode region and the shared floating diffusion region are reset, and prior to the end of the frame period.

31. (original) An integrated circuit, comprising:

a substrate, said substrate having a floating diffusion region;

a first photodiode region formed in said substrate, said first photodiode region having a first light sensitivity characteristic, said first photodiode region being coupled to the floating diffusion region through a transfer transistor formed on said substrate;

a readout circuit formed on said substrate, said readout circuit being coupled to the floating diffusion region;

a second photodiode region formed on said substrate having a second light sensitivity, said photodiode region being coupled to the floating diffusion region through a connecting transistor formed on said substrate; and

a capacitive element formed on said substrate, said capacitive element being coupled to the second photodiode region, and further coupled to the readout circuit.

32. (currently amended) The integrated circuit of claim 31, wherein the readout circuit comprises a reset transistor formed on said substrate, said reset transistor being ~~controllable to reset~~ configured for resetting the floating diffusion region.

33. (original) The integrated circuit of claim 32, wherein the readout circuitry further comprises a source-follower transistor formed on said substrate, said source-follower transistor having a source terminal coupled to said capacitive element, a gate terminal coupled to the drain terminal of the reset transistor, and a drain terminal coupled to a source terminal of a select transistor formed on said substrate, said select transistor having a gate terminal coupled to a select line, and a drain terminal coupled to an output bus line.

34. (original) The integrated circuit of claim 31, wherein the capacitive element is a poly-insulator-poly type capacitor.

35. (original) The integrated circuit of claim 34, wherein the capacitance of said capacitor is in the range of 5 $fF/\mu m^2$ to 10 $fF/\mu m^2$.

36. (original) The integrated circuit of claim 31, wherein the first sensitivity is higher than the second sensitivity.

37. (original) The integrated circuit of claim 31, wherein the capacitance of the floating diffusion region is less than the capacitance of the capacitive element.

38. (original) The integrated circuit of claim 31, wherein the first and second photodiode regions comprise pinned photodiodes.

39. (original) The integrated circuit according to claim 38, wherein the pinned potential is less than 1 volt.

40. (original) The integrated circuit of claim 31, wherein the first and second photodiode regions comprise buried photodiodes.

41. (original) The integrated circuit of claim 31, further comprising:

a third photodiode region formed on said substrate having the first light sensitivity, said third photodiode region being coupled to a second floating diffusion region formed on said substrate through a second transfer transistor, said second floating diffusion region being coupled to the floating diffusion region;

a fourth photodiode region formed on said substrate having the second light sensitivity, said fourth photodiode region being coupled to the second floating diffusion region through a second connecting transistor; and

a second capacitive element formed on said substrate, said second capacitive element being coupled to the second low-sensitivity photodiode region, and further coupled to the readout circuit.

42. (original) A processing system, comprising:

a processor;

an imaging circuit coupled to said processor, said imaging circuit having a pixel circuit, said pixel circuit comprising:

a first photodiode region having a first light sensitivity , said photodiode region being coupled to a first floating diffusion region through a transfer transistor;

a readout circuit, said readout circuit being coupled to the first floating diffusion region;

a second photodiode region having a second light sensitivity, said photodiode region being coupled to the first floating diffusion region through a connecting transistor; and

a capacitive element, said capacitive element being coupled to the second photodiode region, and further coupled to the readout circuit.

43. (currently amended) The processing system of claim 42, wherein the readout circuit comprises a reset transistor, said reset transistor being ~~controllable to reset~~ configured for resetting the first floating diffusion region.

44. (original) The processing system of claim 43, wherein the readout circuitry further comprises a source-follower transistor, said source-follower transistor having a source terminal coupled to said capacitive element, a gate terminal coupled to the drain terminal of the reset transistor, and a drain terminal coupled to a source terminal of a select transistor, said select transistor having a gate terminal coupled to a select line, and a drain terminal coupled to an output bus line.

45. (original) The processing system of claim 42, wherein the capacitive element is a poly-insulator-poly type capacitor.

46. (original) The processing system of claim 45, wherein the capacitance of said capacitor is in the range of 5 $fF/\mu m^2$ to 10 $fF/\mu m^2$.

47. (original) The processing system of claim 42, wherein the first sensitivity is higher than the second sensitivity.

48. (original) The processing system of claim 42, wherein the capacitance of the first floating diffusion region is less than the capacitance of the capacitive element.

49. (original) The processing system of claim 42, wherein the first and second photodiode regions comprise pinned photodiodes.

50. (original) The processing system according to claim 49, wherein a pinned potential is less than 1 volt.

51. (original) The processing system of claim 42, wherein the first and second photodiode regions comprise buried photodiodes.

52. (original) The processing system of claim 42, further comprising:

a third photodiode region having the first light sensitivity, said third photodiode region being coupled to a second floating diffusion region through a second transfer transistor, said second floating diffusion region being coupled to the first floating diffusion region;

a fourth photodiode region having the second light sensitivity, said fourth photodiode region being coupled to the second floating diffusion region through a second connecting transistor; and

a second capacitive element, said second capacitive element being coupled to the second low-sensitivity photodiode region, and further coupled to the readout circuit.